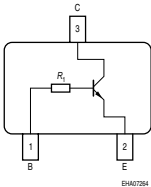


**NPN Silicon Digital Transistor**

- Switching circuit, inverter, interface circuit, driver circuit
- Built in bias resistor ( $R_1 = 47\text{ k}\Omega$ )


**BCR149F/L3  
BCR149T**


Type	Marking	Pin Configuration						Package
BCR149F*	UAs	1=B	2=E	3=C	-	-	-	TSFP-3
BCR149L3*	UA	1=B	2=E	3=C	-	-	-	TSLP-3-4
BCR149T*	UA	1=B	2=E	3=C	-	-	-	SC75

\* Preliminary

**Maximum Ratings**

Parameter	Symbol	Value	Unit
Collector-emitter voltage	$V_{CEO}$	50	V
Collector-base voltage	$V_{CBO}$	50	
Input forward voltage	$V_{i(fwd)}$	80	
Input reverse voltage	$V_{i(rev)}$	5	
Collector current	$I_C$	70	mA
Total power dissipation- BCR149F, $T_S \leq 128^\circ\text{C}$ BCR149L3, $T_S \leq 135^\circ\text{C}$ BCR149T, $T_S \leq 109^\circ\text{C}$	$P_{tot}$	250 250 250	mW
Junction temperature	$T_j$	150	°C
Storage temperature	$T_{stg}$	-65 ... 150	

**Thermal Resistance**

Parameter	Symbol	Value	Unit
Junction - soldering point <sup>1)</sup>	$R_{thJS}$		K/W
BCR149F		≤ 90	
BCR149L3		≤ 60	
BCR149T		≤ 165	

**Electrical Characteristics at  $T_A = 25^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit
		min.	typ.	max.	

**DC Characteristics**

Collector-emitter breakdown voltage $I_C = 100 \mu\text{A}, I_B = 0$	$V_{(BR)CEO}$	50	-	-	V
Collector-base breakdown voltage $I_C = 10 \mu\text{A}, I_E = 0$	$V_{(BR)CBO}$	50	-	-	
Collector-base cutoff current $V_{CB} = 40 \text{V}, I_E = 0$	$I_{CBO}$	-	-	100	nA
Emitter-base cutoff current $V_{EB} = 5 \text{V}, I_C = 0$	$I_{EBO}$	-	-	100	nA
DC current gain <sup>2)</sup> $I_C = 5 \text{mA}, V_{CE} = 5 \text{V}$	$h_{FE}$	120	-	630	-
Collector-emitter saturation voltage <sup>2)</sup> $I_C = 10 \text{mA}, I_B = 0.5 \text{mA}$	$V_{CEsat}$	-	-	0.3	V
Input off voltage $I_C = 100 \mu\text{A}, V_{CE} = 5 \text{V}$	$V_{i(off)}$	0.4	-	0.8	
Input on voltage $I_C = 2 \text{mA}, V_{CE} = 0.3 \text{V}$	$V_{i(on)}$	0.5	-	1.5	
Input resistor	$R_1$	32	47	62	k $\Omega$

**AC Characteristics**

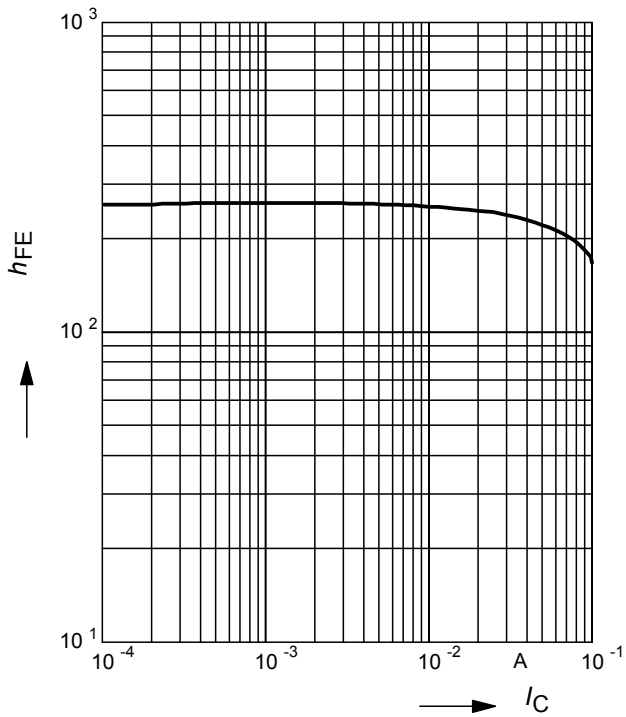
Transition frequency $I_C = 10 \text{mA}, V_{CE} = 5 \text{V}, f = 100 \text{MHz}$	$f_T$	-	150	-	MHz
Collector-base capacitance $V_{CB} = 10 \text{V}, f = 1 \text{MHz}$	$C_{cb}$	-	3	-	pF

<sup>1</sup>For calculation of  $R_{thJA}$  please refer to Application Note Thermal Resistance

<sup>2</sup>Pulse test:  $t < 300 \mu\text{s}; D < 2\%$

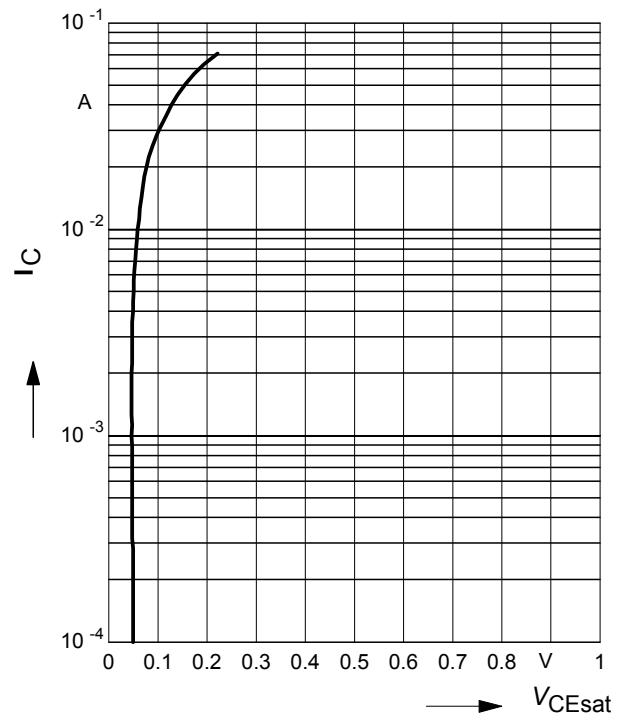
**DC current gain  $h_{FE} = f(I_C)$**

$V_{CE} = 5\text{ V}$  (common emitter configuration)



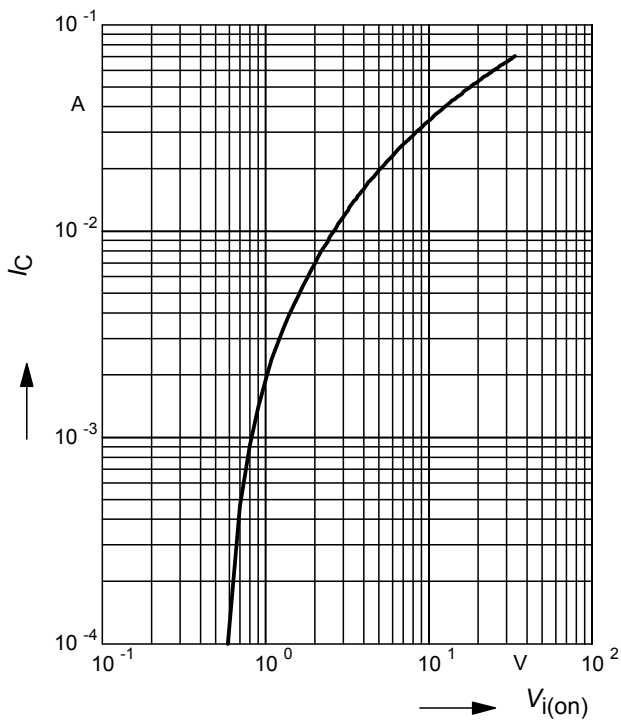
**Collector-emitter saturation voltage**

$V_{CEsat} = f(I_C), h_{FE} = 20$



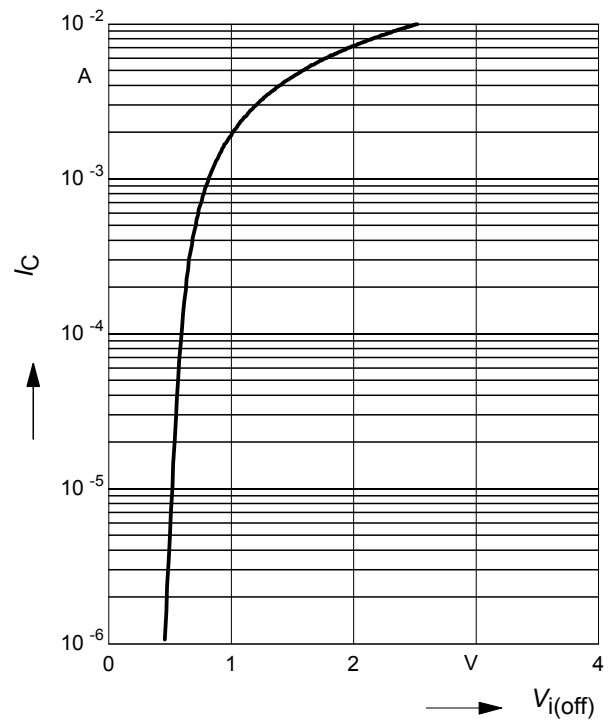
**Input on Voltage  $V_{i(on)} = f(I_C)$**

$V_{CE} = 0.3\text{ V}$  (common emitter configuration)



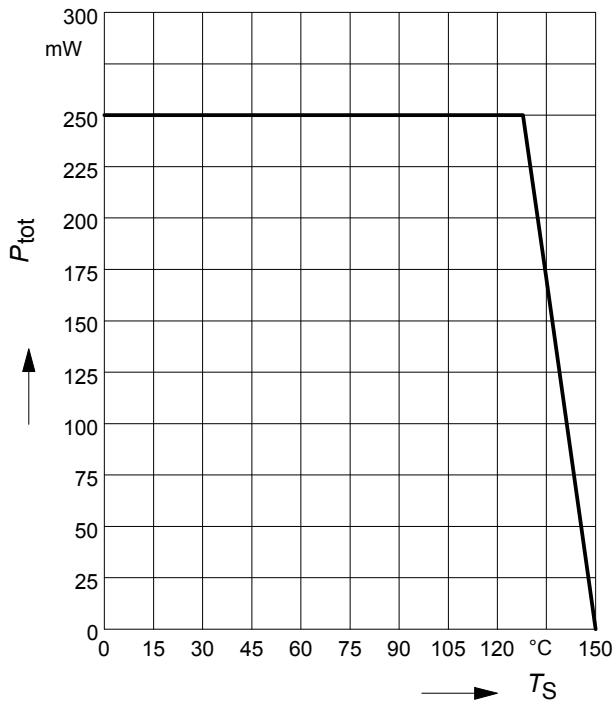
**Input off voltage  $V_{i(off)} = f(I_C)$**

$V_{CE} = 5\text{ V}$  (common emitter configuration)



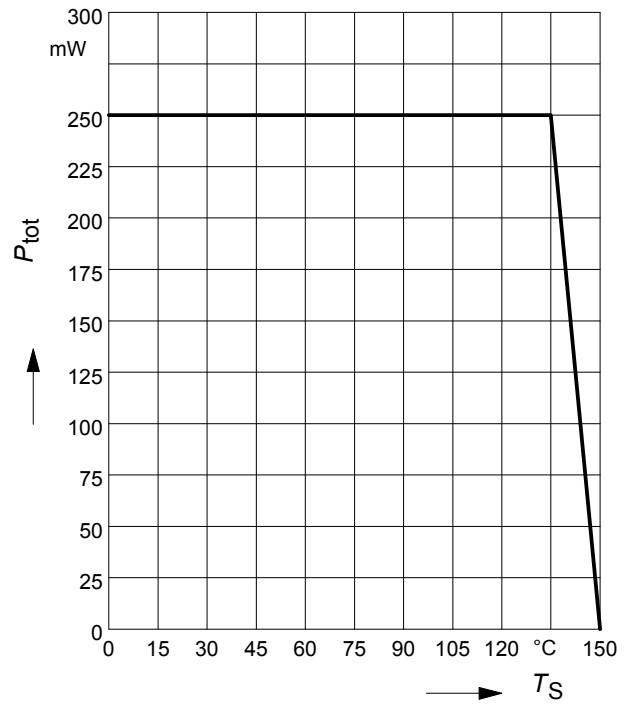
Total power dissipation  $P_{\text{tot}} = f(T_S)$

BCR149F



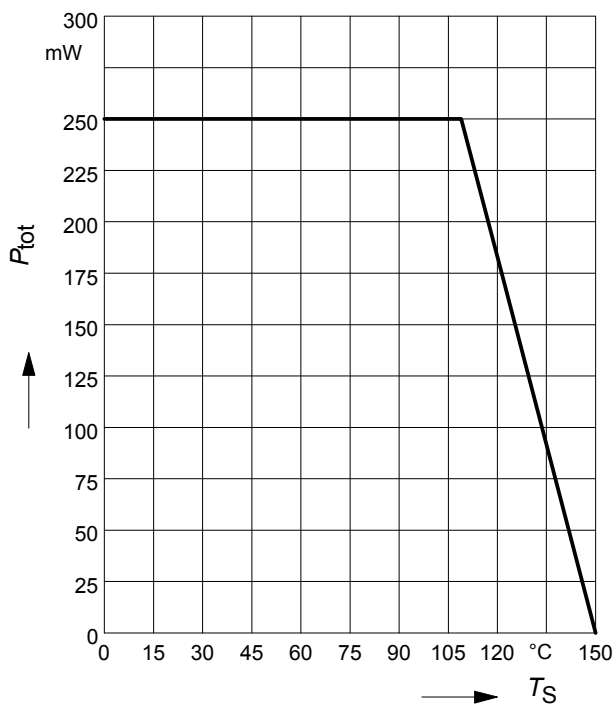
Total power dissipation  $P_{\text{tot}} = f(T_S)$

BCR149L3



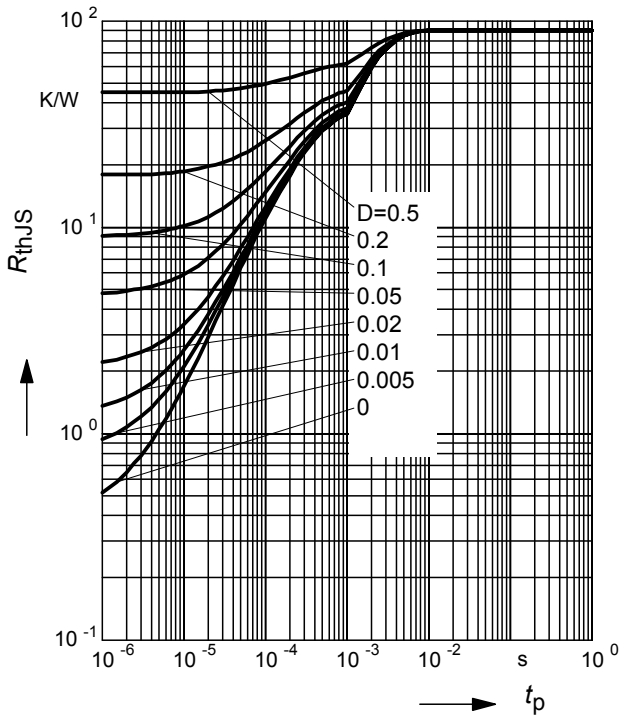
Total power dissipation  $P_{\text{tot}} = f(T_S)$

BCR149T



**Permissible Puls Load  $R_{thJS} = f(t_p)$**

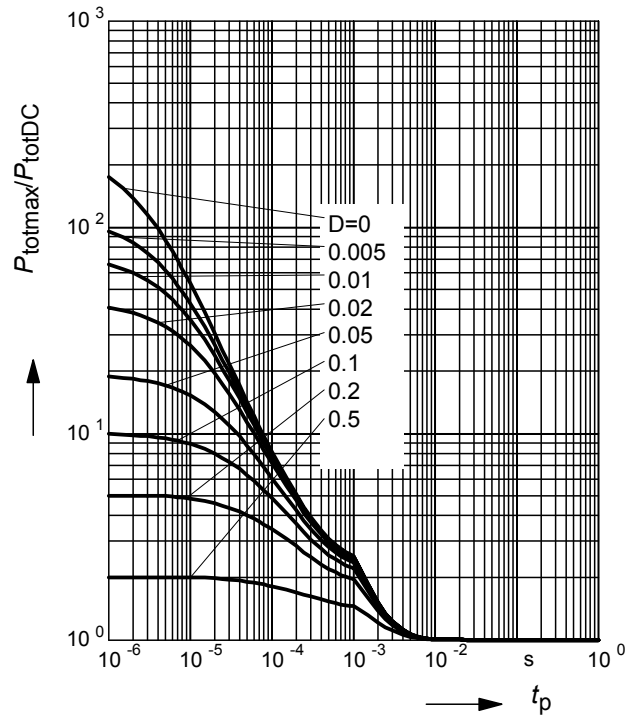
BCR149F



**Permissible Pulse Load**

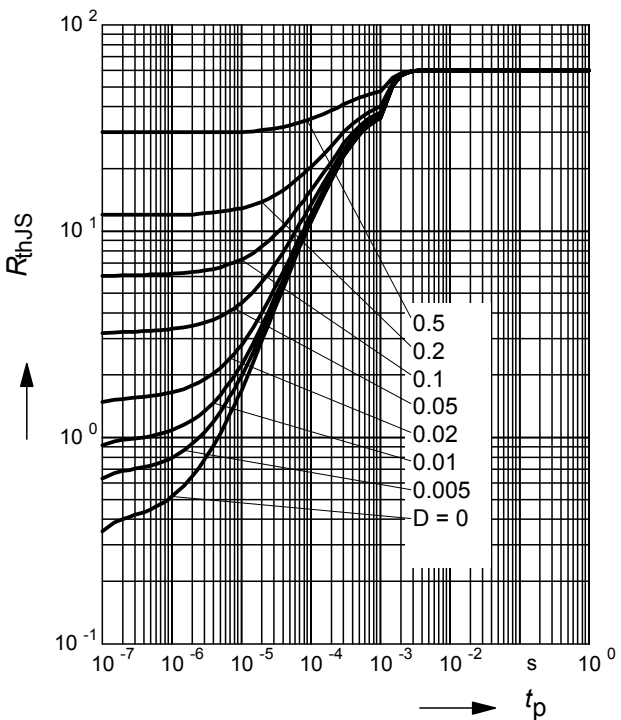
$P_{totmax}/P_{totDC} = f(t_p)$

BCR149F



**Permissible Puls Load  $R_{thJS} = f(t_p)$**

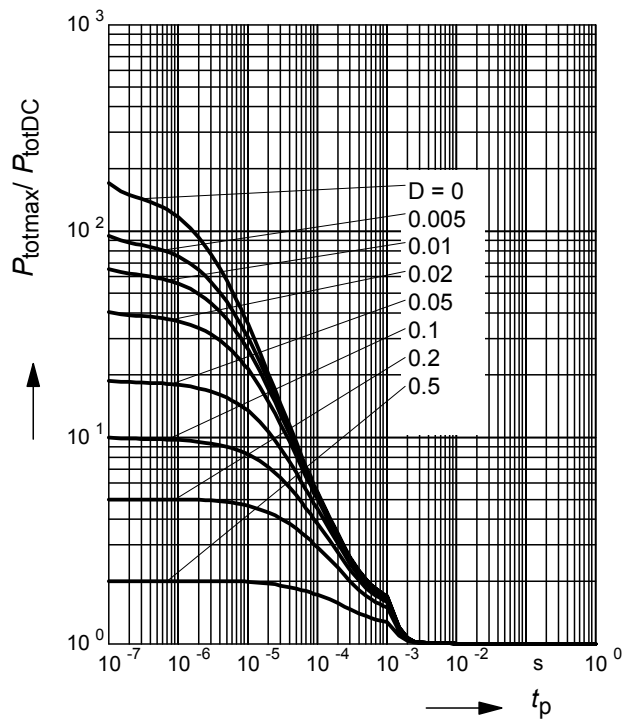
BCR149L3



**Permissible Pulse Load**

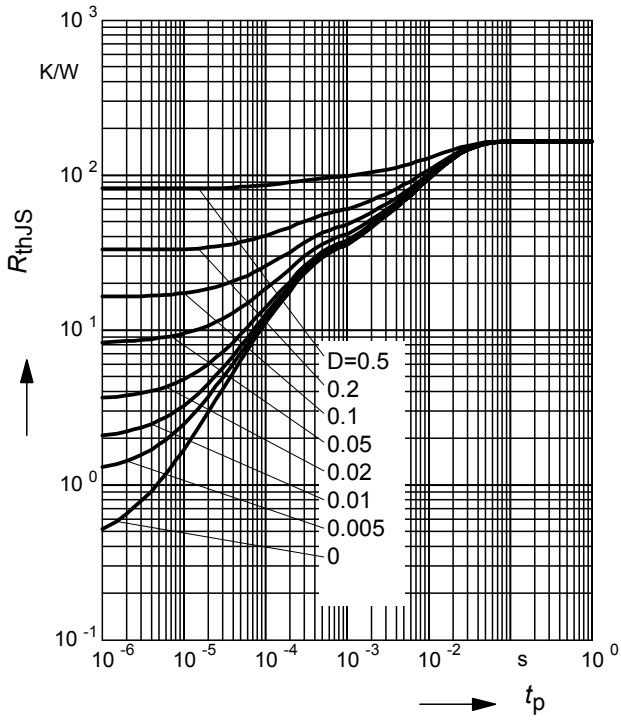
$P_{totmax}/P_{totDC} = f(t_p)$

BCR149L3



**Permissible Puls Load  $R_{thJS} = f(t_p)$**

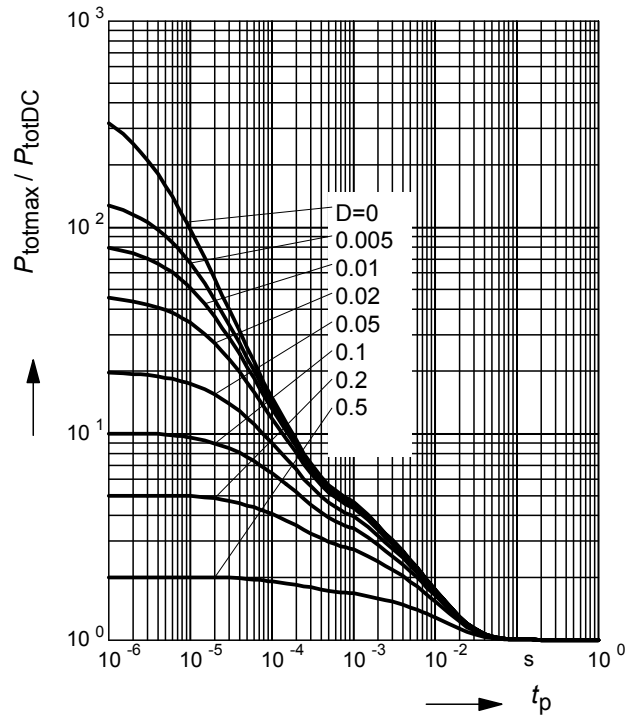
BCR149T



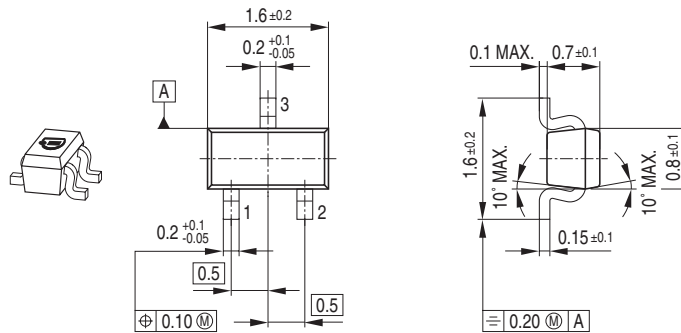
**Permissible Pulse Load**

$P_{totmax}/P_{totDC} = f(t_p)$

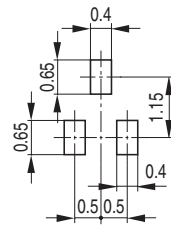
BCR149T



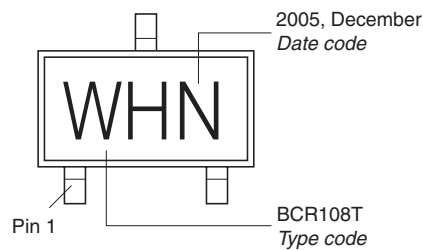
Package Outline



Foot Print

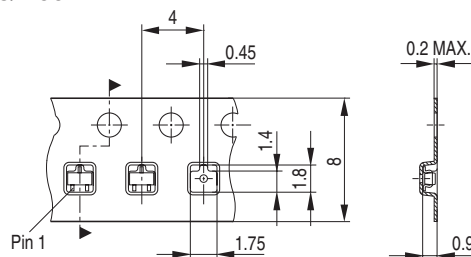


Marking Layout (Example)



Standard Packing

Reel  $\phi 180 \text{ mm} = 3.000 \text{ Pieces/Reel}$   
 Reel  $\phi 330 \text{ mm} = 10.000 \text{ Pieces/Reel}$



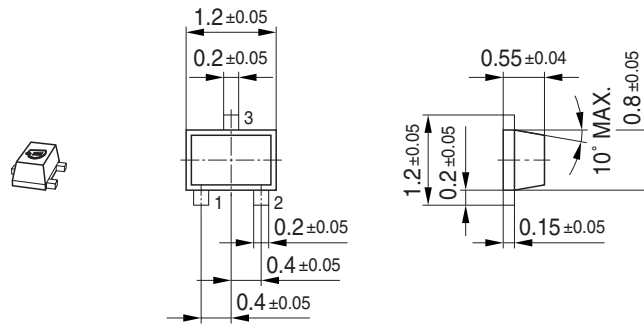
Date Code marking for discrete packages with one digit (SCD80, SC79, SC75<sup>1)</sup>) CES-Code

Month	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
01	a	p	A	P	a	p	A	P	a	p	A	P
02	b	q	B	Q	b	q	B	Q	b	q	B	Q
03	c	r	C	R	c	r	C	R	c	r	C	R
04	d	s	D	S	d	s	D	S	d	s	D	S
05	e	t	E	T	e	t	E	T	e	t	E	T
06	f	u	F	U	f	u	F	U	f	u	F	U
07	g	v	G	V	g	v	G	V	g	v	G	V
08	h	x	H	X	h	x	H	X	h	x	H	X
09	j	y	J	Y	j	y	J	Y	j	y	J	Y
10	k	z	K	Z	k	z	K	Z	k	z	K	Z
11	l	2	L	4	l	2	L	4	l	2	L	4
12	n	3	N	5	n	3	N	5	n	3	N	5

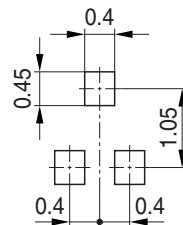
1) New Marking Layout for SC75, implemented at October 2005.



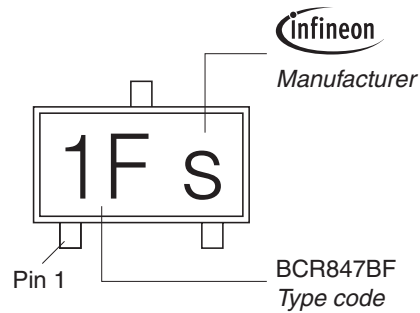
Package Outline



Foot Print



Marking Layout (Example)

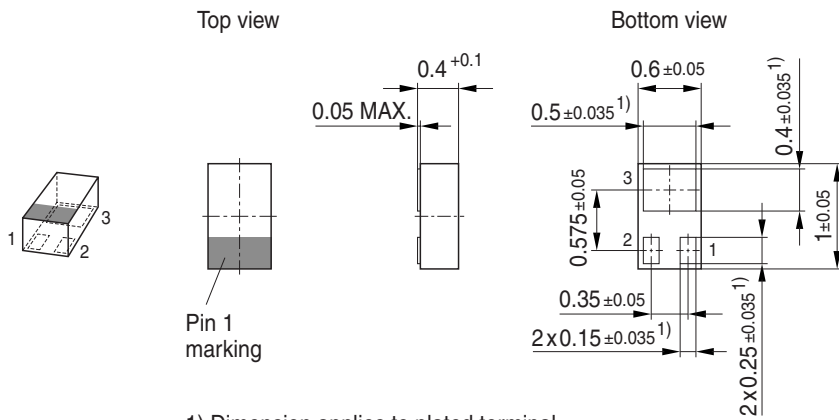


Standard Packing

Reel  $\varnothing$ 180 mm = 3.000 Pieces/Reel  
 Reel  $\varnothing$ 330 mm = 10.000 Pieces/Reel



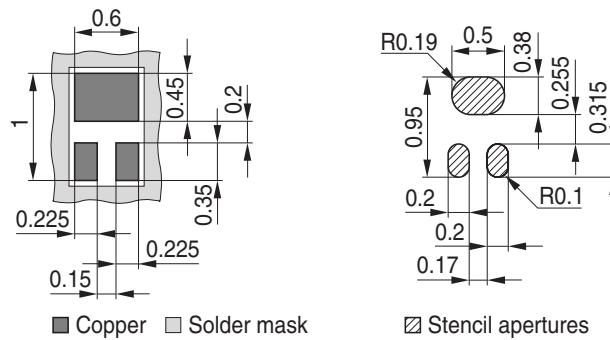
### Package Outline



1) Dimension applies to plated terminal

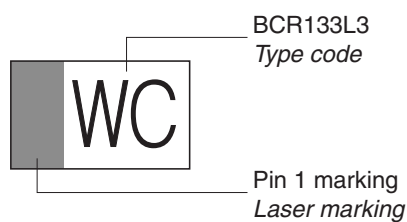
### Foot Print

For board assembly information please refer to Infineon website "Packages"



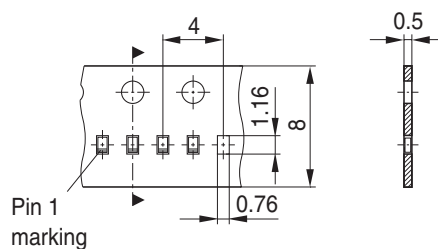
■ Copper □ Solder mask ▨ Stencil apertures

### Marking Layout



### Standard Packing

Reel ø180 mm = 15.000 Pieces/Reel



Edition 2006-02-01

Published by

Infineon Technologies AG

81726 München, Germany

© Infineon Technologies AG 2006.

All Rights Reserved.

### **Attention please!**

The information given in this dokument shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie"). With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

### **Information**

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

### **Warnings**

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system.

Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.